Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A phase error detecting circuit for use in extracting, based on reproduced data that has been reproduced from a record reproducing apparatus and quantized, a synchronous clock which is synchronized with the reproduced data,

the reproduced data being data sampled and quantized by a not-yet-synchronized clock which is not yet adjusted to have a frequency of the synchronous clock,

the phase error detecting circuit comprising:

a cross detector for receiving the reproduced data sampled by the not-yet-synchronized clock and a specified reference value and detecting a cross timing at which the reproduced data sampled by the not-yet-synchronized clock crosses the reference value;

a phase error calculator for receiving the reproduced data sampled by the not-yet-synchronized clock and a cross timing signal from the cross detector and calculating a difference between the value of the reproduced data sampled by the not-yet-synchronized clock and a zero value at the cross timing as phase error data including a phase error amount resulted from a frequency error between the synchronous clock and the not-yet-synchronized clock; and

a cross reference value generator for receiving the phase error data from the phase error calculator and updating the reference value of the cross detector based on the phase error data ~~so that a zero cross point where the reproduced data crosses a zero value is detected with accuracy even when a frequency error between a frequency of the reproduced data and a frequency of a sampling clock for sampling the reproduced data is great~~.

2. (Original) The phase error detecting circuit of claim 1, wherein the cross reference value generator updates, every time the phase error calculator calculates the phase error data, the calculated latest phase error data as the reference value for the cross detector.

3. (Original) The phase error detecting circuit of claim 1, wherein the cross detector has:

a rising cross detector for detecting a rising cross timing at which the reproduced data crosses the reference value upon rising thereof; and

a falling cross detector for detecting a falling cross timing at which the reproduced data crosses the reference value upon falling thereof.

4. (Original) The phase error detecting circuit of claim 3, wherein the phase error calculator calculates, upon receipt of a rising cross timing signal from the rising cross detector, a difference between the value of the reproduced data and the reference value at the rising cross timing as rising phase error data and calculates, upon receipt of a falling cross timing signal from the falling cross detector, a difference between the value of the reproduced data and the reference value at the falling cross timing as falling phase error data.

5. (Original) The phase error detecting circuit of claim 4, wherein the cross reference value generator receives the rising phase error data and the falling phase error data each from the phase error calculator and outputs the rising phase error data as a rising reference value to the rising cross detector, while outputting the falling phase error data as a falling reference value to the falling cross detector.

6. (Original) The phase error detecting circuit of claim 4, wherein the cross reference value generator receives the rising phase error data from the phase error calculator, outputs the rising phase error data as a rising reference value to the rising cross detector, and outputs rising phase error data obtained by inverting the sign of the rising phase error data as a falling reference value to the falling cross detector.

7. (Original) The phase error detecting circuit of claim 4, wherein the cross reference value generator receives the falling phase error data from the phase error calculator, outputs falling phase error data obtained by inverting the sign of the falling phase error data as a rising reference value to the rising cross detector, and outputs the falling phase error data as a falling reference value to the falling cross detector.

8. (Original) The phase error detecting circuit of claim 4, wherein the cross reference value generator receives the rising phase error data and the falling phase error data from the phase error calculator, calculates a 1/2 value of a sum of the inputted rising phase error data and falling phase error data, and outputs the 1/2 value of the sum and a value obtained by inverting the sign of the 1/2 value of the sum as a rising reference value and a falling reference value to the rising cross detector and to the falling cross detector.

9. (Previously Presented) The phase error detecting circuit of claim 1, wherein the cross reference value generator has a structure which fixes the reference value for the cross detector to zero, the phase error detecting circuit further comprising:

a control signal generator for outputting a control signal to the cross reference value generator such that switching is performed between updating of the reference value based on the phase error data and the fixing of the reference value to zero in the cross reference value generator.

10. (Original) The phase error detecting circuit of claim 9, wherein the control signal generator receives the phase error data from the phase error calculator and generates the control signal such that switching is performed between the updating of the reference value based on the phase error data and the fixing of the reference value to zero in the cross reference value generator depending on a phase error shown by the phase error data.

11. (Original) The phase error detecting circuit of claim 10, wherein the control signal generator outputs a control signal such that, when the phase error shown by the received phase error data becomes less than a specified value and approaching a steady state, the generation of the reference value is switched from the updating of the reference value based on the phase error data to the fixing of the reference value to zero.

12. (Original) The phase error detecting circuit of claim 10, wherein the control signal generator generates the control signal such that the reference value is updated based on the phase error data when the phase error shown by the received phase error data is not less than a specified threshold and that the reference value is fixed to zero when the phase error shown by the received phase error data is less than the specified threshold.

13. (Original) The phase error detecting circuit of claim 9, wherein the control signal generator receives a specified signal from an outside of the phase error detecting circuit and generates the control signal such that switching is performed between the updating of the reference value based on the phase error data and the fixing of the reference value to zero in the cross reference value generator in accordance with the specified signal from the outside.

14. (Original) The phase error detecting circuit of claim 13, wherein the control signal generator outputs the control signal such that the generation of the reference value is switched from the updating of the reference value based on the phase error data to the fixing of the reference value to zero upon receipt of a signal which is outputted when a specified pattern of the reproduced data is detected as the specified signal from the outside.

15. (Original) The phase error detecting circuit of claim 14, wherein the signal which is outputted when the specified pattern of the reproduced signal is detected is a sink detection signal which is generated upon detection of a spacing between sink marks in an optical disk.

16. (Original) The phase error detecting circuit of claim 9, wherein the control signal generator receives an abnormal detection signal which is generated when an abnormality occurs in the reproduced data and resets the reference value which is updated based on the phase error data in the cross reference value generator to a specified value.

17. (Original) The phase error detecting circuit of claim 9, wherein the control signal generator receives the phase error data from the phase error calculator and a specified signal

from an outside of the phase error detecting circuit and generates the control signal such that switching is performed between the updating of the reference value based on the phase error data and the fixing of the reference value to zero in the cross reference value generator in accordance with the phase error shown by the phase error data and with the specified signal from the outside.

18. (Original) A synchronous clock extracting circuit comprising:

a phase error detecting circuit as recited in claim 1; and

a voltage control oscillator for receiving the phase error data outputted from the phase error detecting circuit and changing a frequency of a synchronous clock in accordance with a phase error shown by the phase error data.

19. (Original) The phase error detecting circuit of claim 1, further comprising:

a threshold generator for generating a threshold used to update the reference value for the cross detector, wherein

the cross reference value generator receives the threshold from the threshold generator and updates the reference value for the cross detector based on the threshold and on the phase error data from the phase error calculator.

20. (Original) The phase error detecting circuit of claim 19, wherein the threshold generator receives the phase error data from the phase error calculator and specified threshold data from an outside and uses the smaller one of an absolute value of the phase error data and an absolute value of the specified threshold data as the threshold.

21. (Original) The phase error detecting circuit of claim 20, wherein the threshold generator generates a threshold for rising cross timing and a threshold for falling cross timing.

22. (Original) The phase error detecting circuit of claim 21, wherein the cross detector has:

a rising cross detector for detecting a rising cross timing at which the reproduced data crosses the reference value upon rising thereof; and

a falling cross detector for detecting a falling cross timing at which the reproduced data crosses the reference value upon falling thereof.

23. (Original) The phase error detecting circuit of claim 22, wherein the phase error calculator receives a rising cross timing signal from the rising cross detector and calculates a difference between the value of the reproduced data and the reference value at the rising cross timing as rising phase error data and receives a falling cross timing signal from the falling cross detector and calculates a difference between the value of the reproduced data and the reference value at the falling cross timing as falling phase error data.

24. (Original) The phase error detecting circuit of claim 23, wherein the cross reference value generator receives the rising phase error data from the phase error calculator and the threshold for rising cross timing from the threshold generator and uses the smaller one of an absolute value of the rising phase error data and an absolute value of the threshold for rising cross timing as a rising reference value and receives the falling phase error data from the phase error calculator and the threshold for falling cross timing from the threshold generator and uses

the smaller one of an absolute value of the falling phase error data and an absolute value of the threshold for falling cross timing as a falling reference value.

25. (Original) The phase error detecting circuit of claim 23, wherein the cross reference value generator receives the rising phase error data from the phase error calculator and the threshold for rising cross timing from the threshold generator and uses the smaller one of an absolute value of the rising phase error data and an absolute value of the threshold for rising cross timing as a rising reference value, while using a value obtained by inverting the sign of the rising reference value as a falling reference value.

26. (Original) The phase error detecting circuit of claim 23, wherein the cross reference value generator receives the falling phase error data from the phase error calculator and the threshold for falling cross timing from the threshold generator and uses the smaller one of an absolute value of the falling phase error data and an absolute value of the threshold for falling cross timing as a falling reference value, while using a value obtained by inverting the sign of the falling reference value as a rising reference value.

27. (Original) The phase error detecting circuit of claim 23, wherein the cross reference value generator has:

an absolute-value-average calculating circuit for calculating an average value of two absolute values which are the smaller one of an absolute value of the rising phase error data from the phase error calculator and an absolute value of the threshold for rising cross timing from the threshold generator and the smaller one of an absolute value of the falling phase error data from

the phase error calculator and an absolute value of the threshold for falling cross timing from the threshold generator and uses the average value of the two absolute values calculated in the absolute-value-average calculating circuit as each of a rising reference value and a falling reference value.

28. (Previously Amended) The phase error detecting circuit of claim 19, wherein the cross reference value generator has, as the reference value for the cross detector, a zero reference value in addition to the reference value based on the threshold from the threshold generator and on the phase error data from the phase error calculator and has a selecting circuit for selecting either one of the zero reference value and the reference value based on the threshold and on the phase error data.

29. (Original) The phase error detecting circuit of claim 28, further comprising:

a control signal generator for generating a control signal such that the selecting circuit of the cross reference value generator is switched to the zero reference value.

30. (Original) The phase error detecting circuit of claim 29, wherein the control signal generator receives the phase error data calculated in the phase error calculator, generates the control signal when the phase error data has converged to be less than a specified value, and outputs the control signal to the selecting circuit of the cross reference value generator.

31. (Original) The phase error detecting circuit of claim 29, wherein, when the record reproducing apparatus is reproducing data from an optical disk, the control signal generator

generates the control signal upon detection of a spacing between sink marks recorded in the optical disk and outputs the control signal to the selecting circuit of the cross reference value generator.

32. (Original) The phase error detecting circuit of claim 19, wherein the threshold generator comprises:

a decremental circuit for gradually decreasing a specified threshold;

a selecting circuit for selecting either one of the specified threshold and a threshold resulting from the decreasing of the specified threshold by the decremental circuit; and

a switching signal generator for generating a switching signal for switching the selecting circuit to a position of the decremental circuit.

33. (Original) The phase error detecting circuit of claim 32, wherein the switching signal generator generates the switching signal when the number of occurrences of zero crossing of the reproduced data is less than a specified value during a specified period and outputs the generated witching signal to the selecting circuit.

34. (Original) The phase error detecting circuit of claim 32, wherein the threshold generator has a selecting circuit for receiving a control signal from an outside and selecting a threshold with a zero value.

35. (Original) The phase error detecting circuit of claim 19, wherein the cross reference value generator has a gain adjusting circuit for adjusting a value of the phase error data from the phase error calculator to a specified multiple of the original value.

36. (Original) A synchronous clock extracting circuit comprising:

a phase error detecting circuit as recited in claim 19 and

a voltage control oscillator for receiving the phase error data outputted from the phase error detecting circuit and changing a frequency of a synchronous clock in accordance with a phase error shown by the phase error data.